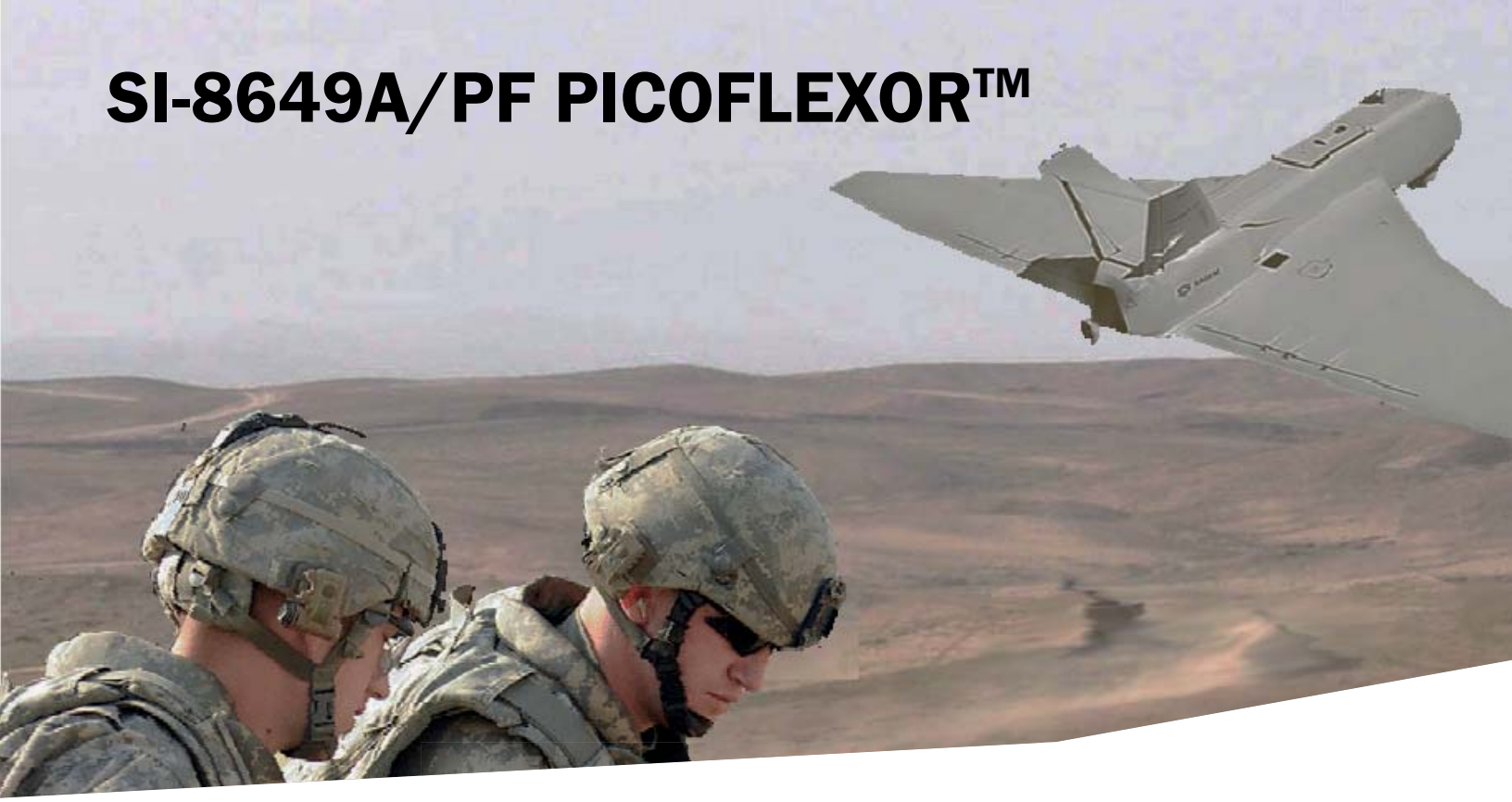
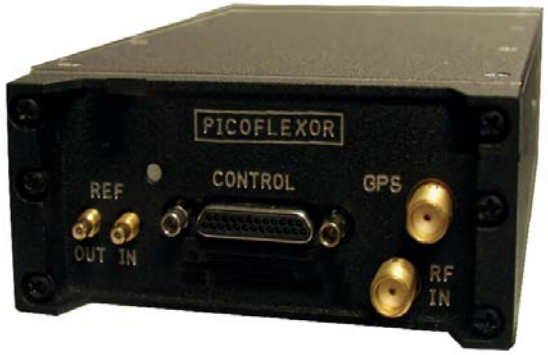
SI-8649A/PF PICOFLEXOR™



SI-8649A/PF PICOFLEXOR™ SOFTWARE DEFINABLE RADIO PLATFORM



PicoFlexor™ is a miniature tactical software definable radio (SDR) platform designed for both application development and deployment in the field. It combines the high RF performance of the Picoceptor™, state-of-the-art digital processing, and a simple development interface to create a best-in-class SIGINT SDR solution.

Its software-definable architecture means that it can be deployed for a signal intercept/analysis application, then re-deployed for threat warning/situation awareness, and again re-deployed to other mission-critical applications, such as precision geo-location or modern signal analysis.

PicoFlexor is designed to rapidly leverage power reduction and performance gains of next-generation digital technology. The architecture is optimized to integrate with open SDR standards such as RedHawk and GNURadio.

KEY FEATURES

- Proven Picoceptor™ RF performance
- Single and dual RF channel configurations
- Phase coherent for N-channel applications
- Precision timing capability for geolocation application
- Removable micro-SD card stores all mission-specific data
- Optional Aft-End-Peripherals provide various I/O standards via high-speed backplane
- Unified tool interface for FPGA and software development
- Common API enables rapid porting of designs across digital technologies
- Digital roadmap includes Xilinx 7-series FPGA and beyond

DRS Technologies
A Finmeccanica Company

SI-8649A/PF PICOFLEXOR™ SOFTWARE DEFINABLE RADIO PLATFORM

PICOFLEXOR™ FAMILY SDR PLATFORM

Tuning Range	2 - 3000 MHz 2 - 12.4 GHz with SI-9249/FE
Channels	Single or Dual
Bandwidth	6 MHz or 25 MHz
Control & Data Interfaces	Gadget mode Ethernet via USB 2.0 USB 2.0 OTG
Control Interface	RS-232

PICOFLEXOR™ DSP MODEL

L1 DIGITAL CONFIGURATION

FPGA	Xilinx Spartan 6 LX45 (45K logic cells)
Processor	TI OMAP DM3730 (ARM Cortex A8 CPU) C64+ DSP core
Memory	512 MB LPDDR-333
Storage	4 GB micro-SD

PICOFLEXOR™ SOC MODEL

S1 DIGITAL CONFIGURATION

SoC	Xilinx ZYNQ 7020 (85K logic cells) Dual ARM Cortex-A9 CPU

S2 DIGITAL CONFIGURATION

SoC	Xilinx ZYNQ 7030[1] (125K logic cells) Dual ARM Cortex-A9 CPU

S1 & S2 COMMON CHARACTERISTICS

Memory	512 MB LPDDR2 (256 MB CPU, 256 MB FPGA)
Storage	4 GB micro-SD

SWAP

Size	
Single-channel	3.0 x 5.7 x 1.3 inches
Dual-channel	3.0 x 5.6 x 1.8 inches
Weight	
Single-channel	<1.5 lbs
Dual-channel	<2.2 lbs
Power Consumption[2] (at 10 Vdc)	/S3B6L1: 4 Watts /D3B6L1: 5.5 Watts /S3B25L1: 5.1 Watts /D3B25L1: 8.4 Watts

INTEGRATED DEVELOPMENT ENVIRONMENT OPTION

The optional Velocity integrated development environment is an Eclipse plug-in that integrates software and FPGA application development, debugging, and deployment functionality into a single graphical environment.

- Allows portability between PicoFlexor models.
- Technology and version agnostic
- Supports rebuilding OS kernels, kernel modules, and file systems for fully customizing for target applications

DEVELOPMENT AEP OPTION

- Ethernet (RJ-45) Control & Data
- JTAG

ORDERING INFORMATION

DSP

SI-8649A/PF/S3B6L1	Single-channel, 6 MHz BW, DSP L1
SI-8649A/PF/D3B6L1	Dual-channel, 6 MHz BW, DSP L1
SI-8649A/PF/S3B25L1	Single-channel, 25 MHz BW, DSP L1
SI-8649A/PF/D3B25L1	Dual-channel, 25 MHz BW, DSP L1

SOC

SI-8649A/PF/S3B6S1	Single-channel, 6 MHz BW, SOC S1
SI-8649A/PF/D3B6S1	Dual-channel, 6 MHz BW, SOC S1
SI-8649A/PF/S3B25S1	Single-channel, 25 MHz BW, SOC S1
SI-8649A/PF/D3B25S1	Dual-channel, 25 MHz BW, SOC S1
SI-8649A/PF/S3B6S2	Single-channel, 6 MHz BW, SOC S2
SI-8649A/PF/D3B6S2	Dual-channel, 6 MHz BW, SOC S2
SI-8649A/PF/S3B25S2	Single-channel, 25 MHz BW, SOC S2
SI-8649A/PF/D3B25S2	Dual-channel, 25 MHz BW, SOC S2

1 Provides enhanced Gigabit Ethernet throughput
2 Based on standard FPGA load; increases with larger loads

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