DRS's SI-8649A SINGLE-CHANNEL HF/VHF/UHF PICOCEPTOR™ SOFTWARE-DEFINABLE RECEIVER

DRS Signal Solutions, Inc.

Meeting Today's Challenges to Provide a Secure Future

Features

- One 2 MHz to 3 GHz RF channel
- Multiple digital drop receivers with AM, FM, CW, PM, USB and LSB detection, and IF filtering from 2 kHz to 200 kHz
- SDR-compatible embedded Linux platform with a field-upgradeable open architecture
- USB 2.0 (OTG) and RS-232 control
- Internal GPS receiver
- Phase-coherent digital IF (I/Q) with time stamping
- User-programmable GPIO lines for custom FPGA loads like antenna control and event triggering
- 1PPS jitter reduction
- Internal calibration signal
- Multiple attenuation tables
- Active antenna bias
- Very low power: < 4.3 W typical
- Compact size 3 x 5 x 0.9 inches (W x L x H) and about 1.0 pound
- MIL-STD-810G rugged, -30 to 80°C (case)

Description

The SI-8649A Single-channel Picoceptor™ is a small, state-of-the-art, single channel, software-definable digital receiver system with a frequency tuning range from 2 MHz to 3 GHz. It provides one analog RF channel and one or two digital drop receivers (DDR) . The Picoceptor can be operated independently or phase-coherently with other SI-8649A receivers. It has narrow-band filtering from 2 kHz to 200 kHz and AM, FM, PM, CW, USB, and LSB demodulation capabilities.

The digital architecture includes Xilinx Virtex-4 SOC (system on a chip) technology that provides an embedded PowerPC and FPGA resources. It runs Linux in an open development environment as a user-managed controller. The USB on-the-go (OTG) interface provides the ability to work with many COTS devices, including storage devices and LAN/WIFI adapters.

The SI-8649A has the dynamic range and distortion performance necessary to intercept weak signals in crowded signal environments.

Tuning Range, Modes, Speed: The SI-8649A tuning range is from 2 MHz to 3 GHz. It can be manually tuned or automatically swept from any F1-F2 within the tuning range. The Picoceptor is equipped with up to 200 channels for sector sweeps and scans, and up to 200 lockout channels. When sweeping, the frequency settling time is less than 500 microseconds from receipt of command to within 1 kHz of final frequency. Additional settling time is required through the DDR and is bandwidth dependent.

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RF Bandwidth, ADC & DDR Characteristics: The SI-8649A has two RF analog bandwidth options (6 and 25 MHz), and seven digital bandwidths ranging from 2 kHz to 200 kHz in octave steps. Each digital bandwidth can be tuned throughout the entire analog bandwidth. In the Picoceptor, digital tuning is also allowed over the entire Nyquist bandwidth (±Fs/4). The standard receiver FPGA load comes with either one or two digital drop receivers determined by selection of the Xilinx FX12 or FX60 FPGA with a range of bandwidths suitable for commercial communication signal formats.

GPS Receiver: The Picoceptor design includes a GPS receiver with a front-panel connector specifically for use with a GPS antenna. The receiver is capable of providing both location information and extremely accurate time information. The latter can be used as a source of time-stamp information as well as a frequency reference. The GPS input connector can also source up to 50 mA of current for an active antenna with a +5.0 Vdc supply.

Phase-Coherent Operation: Rather than share LO signals among channels in a phase-coherent system, the SI-8649A master unit modulates its output reference signal with information which is used to synchronize other Picoceptors in a multi-channel array. Simply daisy chaining the 10 MHz reference from one unit to another greatly reduces the amount of cabling and the cost associated with running high frequency cables throughout the system. For units that are not co-located the Picoceptor features an application that permits synchronization using a GPS input as a reference.

Reference Options: The SI-8649A can operate on its own internal 10 MHz, low jitter, 1 part per million (1ppm) frequency stable reference, or an external 1 pulse per second (1PPS) or external 10 MHz source. The 1PPS source can either be received from the input reference connector or the 25 pin micro-D front panel connector. In a master/slave mode 1PPS can be encoded onto the 10 MHz from the master and decoded on each slave channel. Each 1PPS is internally routed to an internal PLL system which locks it to the internal 10 MHz and provides jitter reduction. The external 10 MHz can only be applied to the reference input.

1PPS Jitter Reduction: When an external 1PPS signal is used as a reference, the SI-8649A reduces jitter by conditioning the signal to stabilize it.

GPIO Lines: There are four general-purpose IO lines connected to the FPGA that can be used as either inputs or outputs to provide customized interface capabilities such as switching antenna elements, indicating COR status, providing audio squelch and blanking functions, or sending/receiving event signals. This feature is provided for use by FPGA developers and is not part of the standard receiver firmware.

Active Antenna Bias: When the SI-8649A is used with an antenna via a long length of cable, this feature provides the ability to power an amplifier located near the antenna without additional bias networks and cabling.

Internal Calibration Signal: The SI-8649A has an internal signal generator connected to the RF input which can be used to test and calibrate the receiver. When activated, the Picoceptor generates spectral frequency components equally spaced by 10 MHz covering the full tuning range of the receiver starting from 10 MHz to 3000 MHz.

Multiple Attenuation Tables: The SI-8649A has three built-in attenuation tables for optimized signal performance in rural, urban and suburban areas. The default table is optimized for Noise Figure (NF), the second for Spur Free Dynamic range (SFDR), and a third allows for a user-defined attenuation table. Each table spans the 0 to 46 dB attenuation range of the Picoceptor and allows RF front-end attenuation (0 – 15 dB) and IF back-end attenuation (0 – 31 dB) to be independently set to maximize performance.

Power: The SI-8649A operates on DC power from 6V to 16V. The optimal voltage for best power efficiency is ~6-7 Vdc. Depending on the analog bandwidth and the Xilinx part installed, the power can range from 4.3 W for a 6 MHz bandwidth unit with an FX12 (S3B6X12) to 7.6 W for a 25 MHz bandwidth unit (S3B25X60). The SI-8649A provides several low-power suspend modes that can be initiated through the control interface so that the unit can be shut down and reactivated remotely to conserve power.

Temperature Range: The SI-8649A's operating temperature range of -30 to +80 °C case temperature enhance its ruggedness and mission reliability.

Onboard System Controller: The embedded PowerPC running Linux provides a platform on which it is relatively

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easy to implement custom applications. Coupled with the USB 2.0 OTG interface and its ability to perform as either host or device, the SI-8649A offers a wide range of operational flexibility. The design contains sufficient RAM and flash memory to support the Linux operating system and most software-definable radio (SDR) operating environments (e.g., JTRS SCA, X Midas, etc.).

USB On-The-Go (OTG): The USB 2.0 OTG interface allows attachment of peripheral devices such as thumb drives, Ethernet devices, GPS receivers and Bluetooth modules. The USB 2.0 interface allows direct, high-speed connectivity to a PC or laptop. This USB standard uses a master/slave architecture in which a USB host acts as the protocol master and a USB device acts as a slave. Only the host can schedule the configuration and data transfers over the link. USB devices can only respond to requests from a host.

OTG introduces the concept that a unit with a USB interface can perform both the master and slave roles (one role at a time). An OTG device can be either a link master or a link slave.

System Architecture: The downloadable architecture of the SI-8649A makes it ideally suited for customer-specific applications. As shown in the detailed block diagram (Figure 1), the unit contains a powerful FPGA (Xilinx Virtex 4) including controller functionality. Other system resources include 64 MB DDR SDRAM and Flash memory and external resources can be accessed through the USB interface. The embedded Linux platform appears to the user as any other PC. In host mode it provides a TCP/IP stack that makes it easy to access peripheral devices.

Users are able to transfer data into the unit via a file transfer protocol (FTP) or a telecommunications network (telnet) protocol, run custom software, and control other units via the serial interface. This allows the Picoceptor to be used as a controller and processing platform for complex DSP applications, where small size and low power provide a critical advantage.

VITA-49 Data: The SI-8649A supports the VITA 49 digital data IF protocol standard, which provides for time-stamping of the digital I&Q data out of the digital drop receiver. This time-stamped data can be used to align data from multiple units in a TDOA or DF application. The VITA 49 FPGA load is a separate FPGA load and is not installed as the standard load.

Digital Data Snapshots: The standard firmware also comes with a built-in digital data snapshot function to allow output of digital IF spectral data for signal monitoring operation. This function gives the user the ability to retrieve ADC, post-CIC filter, or post-demodulated data. This building block can be used as a foundation for high-speed signal searches, new energy detection, or an IF panoramic display.

Customer Training: A developer class is available to support customers interested in creating custom solutions.

Optional Software Loads: Instead of the standard narrow-band surveillance receiver software load, other software loads are available for wideband tuning, new energy detection, and high-speed scanning. Availability is FPGA-dependent. Contact the factory for information.

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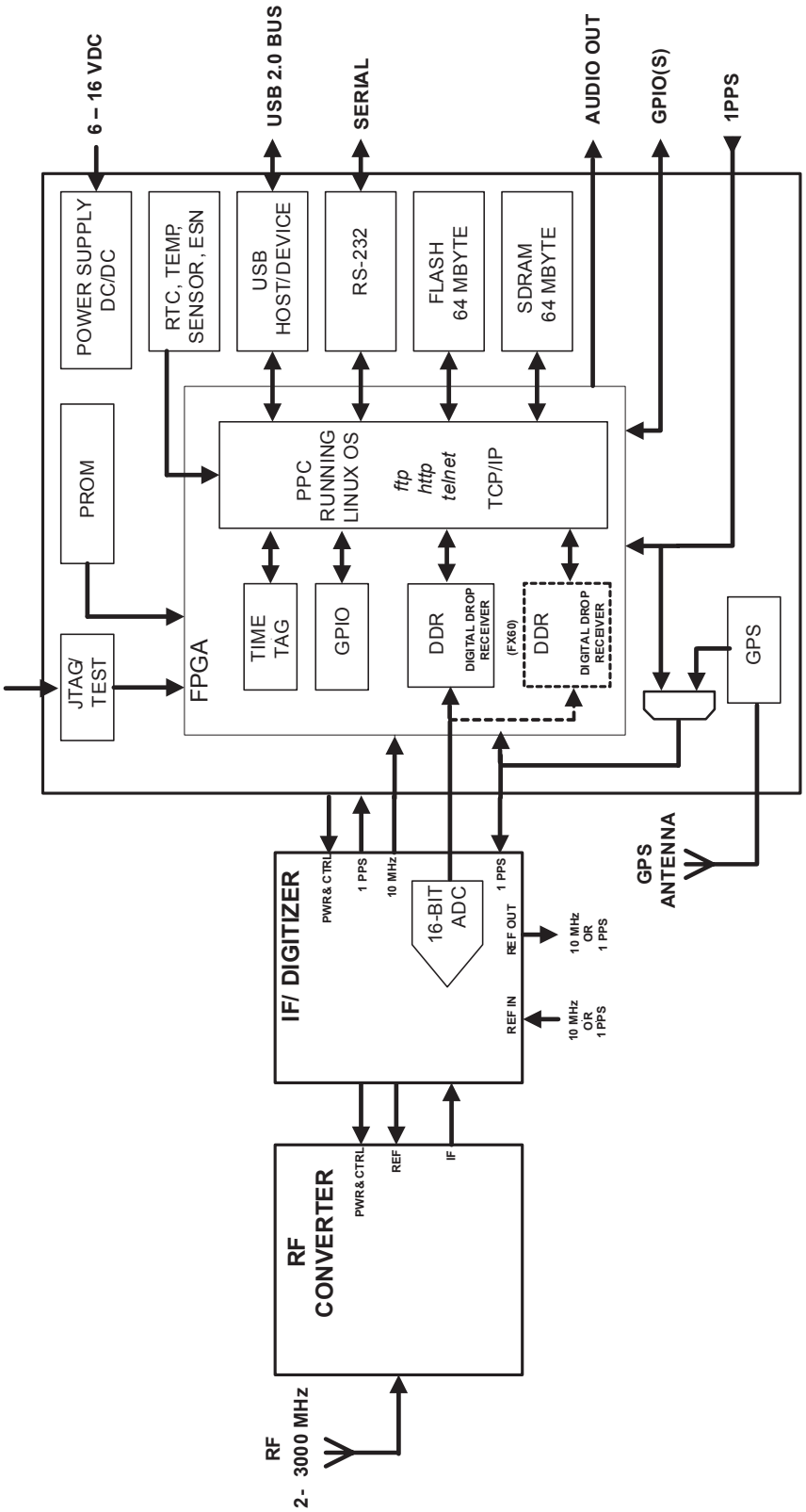

Figure 1. Functional Block Diagram of Single-Channel Picoceptor

Parameter	Specification
Frequency range	
Tuning range	2 MHz to 3000 MHz
Specification compliant range	30 MHz to 3000 MHz
Tuning resolution	1 Hz
Tuning speed	Less than 500 microseconds from receipt of command to within 1 kHz of final frequency in sweep/scan mode
Internal frequency stability	±1.0 ppm
External reference frequency input	10 MHz, 0 dBm ±10 dB 1PPS, 3.3V TTL/CMOS, 4.0V maximum, 50% duty cycle
Phase Coherence	Multi-channel phase-coherent operation is accomplished by distributing the 10 MHz reference output from the Master to other Slave units in the chain
Preselection	
Bypass mode	Low-pass filter with 200 MHz bandwidth
20 to 459 MHz	Tracking filters (30% 3 dB bandwidth)
459 to 3000 MHz	Switched sub-octave filters
Noise figure	
2 to 30 MHz	15 dB typical @20 MHz, higher below 20 MHz
30 MHz to 2.7 GHz	11 dB typical, 15 dB maximum
2.7 GHz to 3 GHz	14 dB typical, 17.5 dB maximum
RF input	
Impedance	50 Ohms
VSWR at tuned frequency	VSWR < 2.0:1 typical, 2.5:1 maximum
Maximum RF input without damage	+30 dBm
Input 3rd-order intercept point	
30 to 1200 MHz	
@ 30 MHz offset	+5 dBm typical, +2 dBm minimum
Within the final IF passband	-5 dBm typical, -8 dBm minimum
1200 to 3000 MHz	
@ 30 MHz offset	+7 dBm typical, +4 dBm minimum
Within the final IF passband	-5 dBm typical, -8 dBm minimum
Input 2nd-order intercept point	
30 to 3000 MHz	+50 dBm typical, +30 dBm minimum
Phase noise	
1 kHz	-83 dBc/Hz typical, -80 dBc/Hz maximum
10 kHz	-85 dBc/Hz typical, -82 dBc/Hz maximum
100 kHz	-104 dBc/Hz typical, -101 dBc/Hz maximum
1 MHz	-134 dBc/Hz typical (***Note 1***)
10 MHz	-153 dBc/Hz typical (***Note 1***)

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Parameter	Specification
RF tuner bandwidth	6 MHz or 25 MHz (***Note 2***)
Gain control	Range sufficient for RF input levels up to +10 dBm
Attenuation	
Analog frontend	0 – 46 dB, 1 dB steps
Digital backend	0 – 84 dB, 6 dB steps
Full-scale input power with no attenuation	
30-2700 MHz	-28 dBm ±4 dB at maximum gain
2700-3000 MHz	-26 dBm ±4 dB at maximum gain
Image rejection	90 dB typical, 80 dB minimum
IF rejection	90 dB typical, 80 dB minimum
LO level at RF input	<-95 dBm typical, -80 dBm maximum
Internally-generated spurious	≤-100 dBm equivalent RF input maximum
Digital drop receiver (DDR)	
Number of channels	
FX12	One
FX60	Two
Digital receiver bandwidths	2 kHz to 200 kHz (***Note 3***)
Tuning range	±4.67 MHz with 1 Hz resolution (***Note 4***)
	±23.333 MHz with 1 Hz resolution (***Note 5***)
Demodulation types	AM, FM, PM, CW, USB and LSB
Internal calibration signal	10 MHz to 3 GHz, 10 MHz steps
Active RF antenna bias	3.0 to 4.5 Vdc, 80 mA maximum
Data interface	USB 2.0 OTG
Data format	VITA-49 compliant, with time stamp (***Note 6***)
Digital IF data type	In-phase/Quadrature phase
DSP processor	Xilinx Virtex 4 FPGA-based. FX12 and FX60 FPGA supports Linux OS and SDR applications (Consult factory for other options)
Global positioning system (GPS)	Internal GPS
Channels	20, parallel tracking
Correlators	200,000 plus
Frequency	1575 MHz
Tracking sensitivity	-159 dBm (***Note 7***)
Position accuracy	< 10m CEP (SA off)
Horizontal position accuracy	< 2.5m CEP (SA off)
Time to first fix - TTFF	35 sec maximum (***Note 8***)
Active antenna bias	4.5 to 5.5 Vdc, 50 mA maximum
Power consumption	4.3 W typical, (***Note 9***)
Power supply	6 – 16 Vdc
Remote control	RS-232 and USB 2.0 OTG supported
Dimensions	3.0 W x 5.0 L x 0.9 H inches
Weight	Approximately 1.0 lbs

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Parameter	***Specification***
Environmental performance	
Specification-compliant temperature range (case)	-20 to +70°C
Operating temperature range (case)	-30 to +80°C (***Note 10***)
Storage temperature range	-40 to +85°C
Altitude	0 - 60,000 ft (MIL-STD-810G, Method 500.5, Procedure II, 40°C)
Humidity	10 to 90% non-condensing (MIL-STD-810G, Method 507.5, Procedure II, Aggravated cycle)
Vibration, operating	MIL-STD-810G, Method 514.6, Category 24, Figure 514.6 E1, minimum integrity test, 1 hour per axis.

NOTES:

(1) Measured at the internal analog final IF frequency.

(2) The SI-8649A Single-channel Picoceptor family of products can include multiple bandwidth options. See the section titled "Single-Channel SI-8649A Ordering Information" for a list of all currently available bandwidth options. Consult the factory for a full list of planned bandwidth options.

(3) Bandwidth choices shown are for the 6 MHz RF BW configuration (in a 2, 5, 10 sequence)
Bandwidth choices for the 25 MHz RF BW are 5 kHz to 200 kHz.

(4) Assumes 6 MHz bandwidth and 18.666666 MSPS ADC sample frequency.

(5) Assumes 25 MHz bandwidth programmed for 93.333337 MSPS ADC sample frequency.

(6) VITA 49 capable FPGA software load shipped separately, consult manual on how to install Vita 49 FPGA load in unit to access time stamp data.

(7) Typical performance with active antenna of >20 dB gain and <1.5 dB noise figure.

(8) Theoretical minimum from a cold start, receiver has no information about date/time/position and recent almanac.

(9) Using a +10 V power supply,

Configuration	Watt (typical)	Watt (maximum)	
S3B6X12	4.3	4.7	These power specifications assume factory default FPGA and software designs. Custom FPGA and software designs may consume additional power. To minimize power consumption, use 6-to-7 V power.
S3B6X60	5.2	5.9	
S3B25X12	5.4	6.1	
S3B25X60	6.3	7.0	

(10) Temperature range for factory-installed FPGA builds. The operating temperature specification refers to the case temperature. Additional cooling may be needed for larger FPGAs with customized FPGA designs.

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Single-Channel SI-8649A Options/Accessories

Options	Description
8649A/PLK Picoceptor Launch Kit	Kit contains: cables, power supply, adaptors, SDR windows based GUI software, training, post sales phone support, getting started guide and operations manual to launch Picoceptor.
Accessories	**Description**
8649/PS	Plug-In Converter Power Supply: Power adapter with a LEMO cable output. Connects to the DC inputs of the 8649/STDCABLES and the 8649/ADVCABLES cable kits.
8649/STDCABLES	Picoceptor SDR Standard Cable Set: Connects to the front panel of any Picoceptor and provides a LEMO connector for DC power, a standard USB receptacle for USB control, a 9-pin standard D connector for RS232 control, and a phone jack for audio output.
8649/ADVCABLELEMO 8649/ADVCABLEBANANA	Picoceptor SDR Advanced Cable Sets: Each includes two sets of cables allowing full access to all inputs/outputs on the SI-8649A's front-panel 25-pin connector. One optional set allows power through a LEMO connector; the second provides power through standard banana plugs.
8649/NOCABLES	This option is selected when no cables are desired.

*Contact factory for additional training and accessory details.

Ancilliary Equipment

SI-9249/FE12	Extends the frequency range of single-channel Picoceptor to 12.4 GHz
9249/FE/SNGLPICOKIT	Kit for FE operation with single-channel SI-8649A. Consists of custom cables, Ethernet adaptors and mounting brackets.

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Key to Option Designations

SI-8649A/***CFB***AA***X***##

SI-8649A/	C	F	BAA	X##
Product Family	***C***hannel count S = Single (1)	Upper ***F***requency (GHz) Options: 3	***B***W option (MHz) Options: 6, 25	***X***ilinx FPGA options X12 = XC4VFX12 X60 = XC4VFX60

Single-Channel SI-8649A Ordering Information

Product Type	Nomenclature	Description
Single-channel, 6 MHz BW, low power	SI-8649A/S3B6X12	Single-channel 6 MHz bandwidth Picoceptor with a Virtex-4 FX12 FPGA. Low power. Medium-low FPGA & DSP resources
Single-channel, 6 MHz BW, high performance	SI-8649A/S3B6X60	Single-channel 6 MHz bandwidth Picoceptor with a Virtex-4 FX60 FPGA. Largest FPGA. Extensive FPGA & DSP resources
Single-channel, 25 MHz BW, low power	SI-8649A/S3B25X12	Single-channel 25 MHz bandwidth Picoceptor with a Virtex-4 FX12 FPGA. Low power. Medium-low FPGA & DSP resources
Single-channel, 25 MHz BW, high performance	SI-8649A/S3B25X60	Single-channel 25 MHz bandwidth Picoceptor with a Virtex-4 FX60 FPGA. Largest FPGA. Extensive FPGA & DSP resources

DRS Signal Solutions, Inc.

700 Quince Orchard Road, Gaithersburg, MD 20878-1794 Tel 1.301.948.7550 Fax 301.921.9479 www.drs.com | SSI_sales@drs.com